ABSTRACT OF THE DISCLOSURE

A number of enhanced logic elements (LEs) are provided to form a FPGA. Each enhanced LE comprises a multiple input-single output truth table, and a complementary pair of master-slave latches having a data, a set and a reset input. Each enhanced LE further comprises a plurality of multiplexers and buffers, and control logic. Additionally, the improved FPGA further comprises a network of crossbars, a context bus, a scan register, and a plurality of trigger circuitry. As a result, each LE may be individually initialized, its signal state frozen momentarily, the frozen state be read, trace data be output, and trigger inputs be conditionally generated. Furthermore, the enhanced LEs may be used for "level sensitive" as well as "edge sensitive" circuit design emulations.